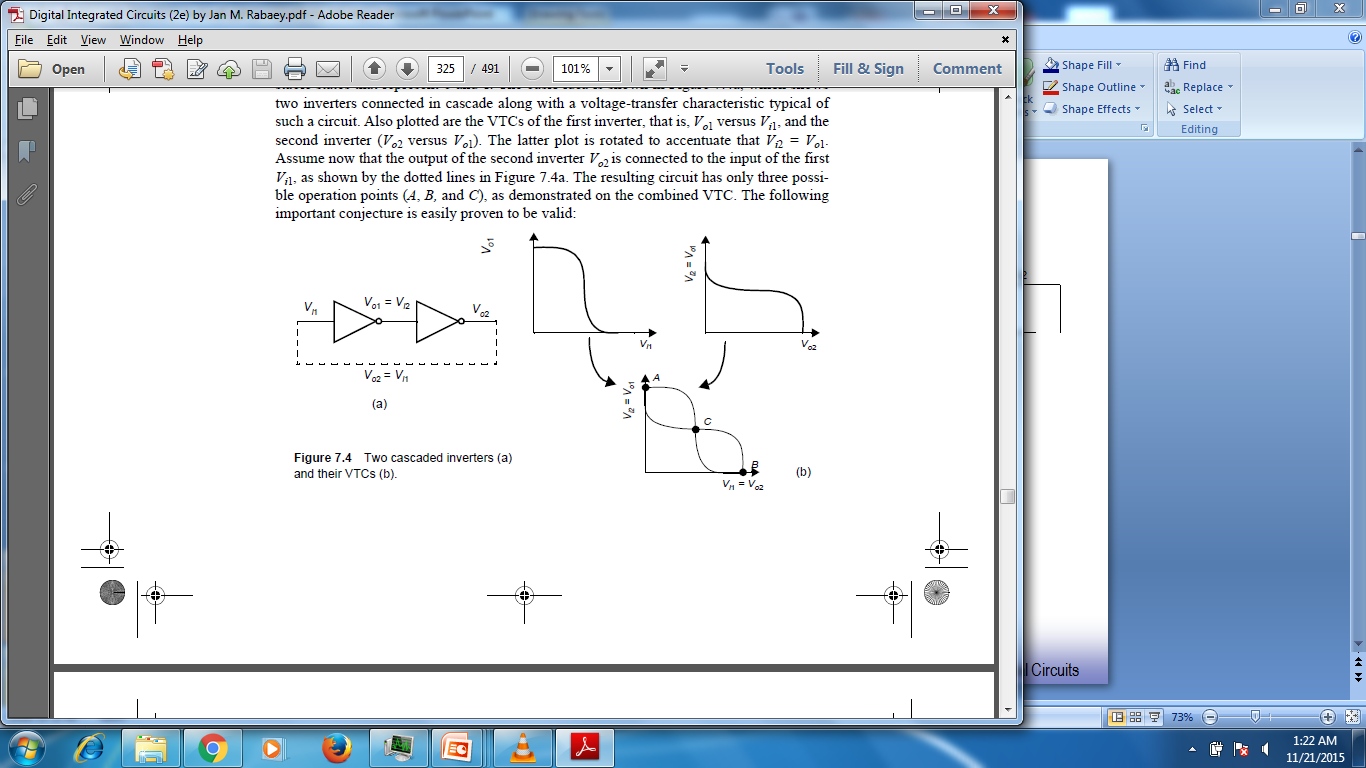
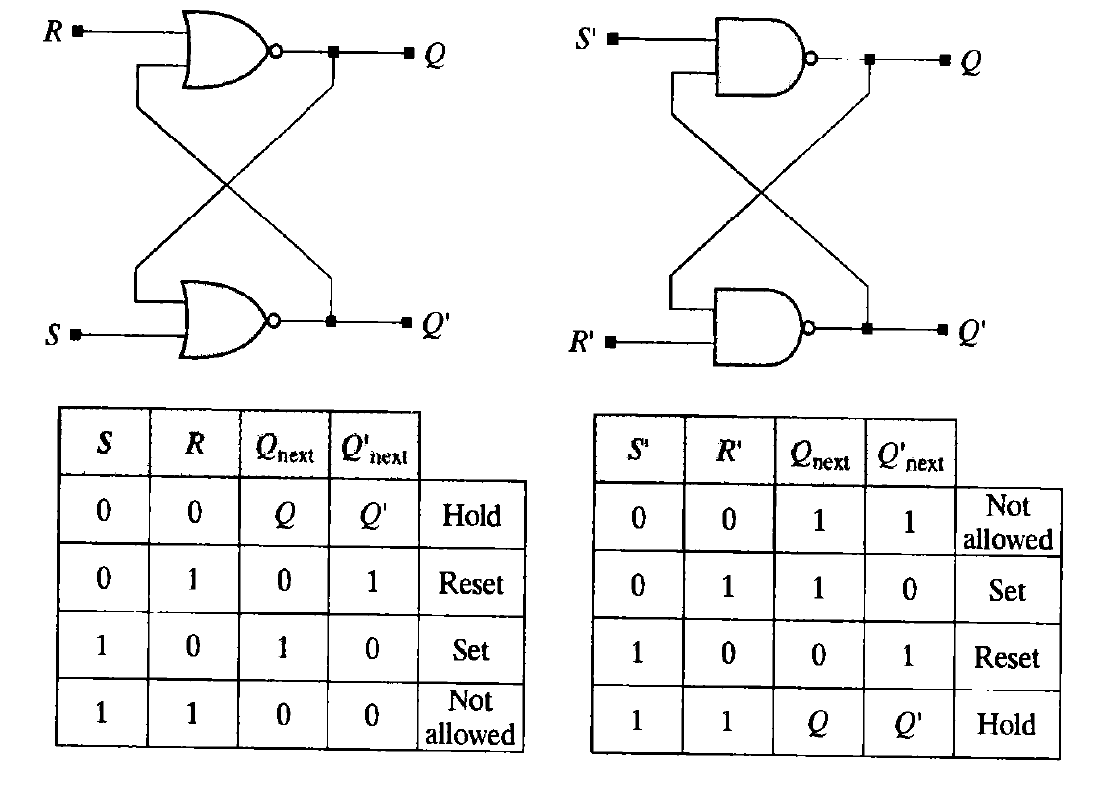
**Question # 1 : [CLO-1]**

Two digital inverters are connected in the back-to-back; input of invert1 is connected to output of inverter2 and output of inverter1 is connected to input of inverter2. You may assume that the input of the first inverter is 0 and the output of the second inverter is 0 as well. Briefly comment what functionality this configuration is achieving and suggest a change in the circuit to provide a trigger to make the circuit change its output state from 0 to 1(VDD) where a low value of trigger should toggle that circuit state and a high value should not affect the existing state. [10]



****

S and R are the triggers. R is redundant here can be removed and therefore the 2nd NAND can be replaced back inverter.

**Question # 2 : [CLO-1]**

Two flip-flops are connected in series with the output of the first flip-flop directly connected to the input of the second. The clock to Q delay of flip-flops is 1nsec. The setup time is 1nsec. The hold time is 1nsec. Calculate the maximum frequency this digital circuit can operate at. [10]

Tc2Q represents the delay to output from first FF after the clock edge. Tsetup represents the early arrival needed at the input of the second FF before the next edge of clock. Thold is satisfied through tc2q.

fmax = 1/Tmax = 1/(tc2Q + tsetup) = 1 / (1n + 1n) = 500MHz

**Question # 4 : [CLO-2]**

You have an NMOS and a resistor, there is no PMOS. Implement a digital inverter and calculate the expressions for tPLH and tPHL. If kn=100uA/V2 and W/L=1 and VDD=5V and VTH=0.5V, calculate exact values of these propagation delays assuming you are driving a capacitive load of a typical digital oscilloscope probe (You may chose to ignore resistive component of the probe) .

[20]

RON\_NMOS = 1/(kn\*VOV\*W/L) = 2.2k ohm

There is a voltage divider between Rpull\_up and RON\_NMOS. For output to go below VDD/2, RON has to be smaller than Rpull-up. Assuming Rpull-up is 2\*2.2k = 4.4k ohm.

Tphl = 0.69\*RON\_NMOS\*CL = 21n sec (approx.)

Accurate method would require the following calcs from VDD to VDD\*2.2/6.6 =1.66V

1.66=5e^-t/RC

t=RC\*ln(1.66/5) = 1.1\*RC = 15.4p \* R = 15.4p \* 2.2k\*4.4k/6.6k = 22n sec

For Tplh = 0.69\*Rpull-up\*CL = 42n sec.

Try changing Rpull-up and try to take tplh and tphl as close as possible.

But as you can see this is an asymmetric circuit and therefore the rise fall times are going to be different.

**Question # 5 : [CLO-2, CLO-3, CLO-4]**

Write Verilog code of a module that implements a 16-bit shift register using cyclic constructs that proper infer flipflops and avoid latches, with and without for-loop constructs. The complete code should be of less than 15 lines. Attach simulation snaps of this code from Xilinx Vivado software.

[20]

…

Always @(posedge clk)

begin

if (reset)

Sreg <= 16’b0;

Else if(enable)

Sreg [15:0 ] <= {Sreg[14:1],data\_in};

End

…

…

Always @(posedge clk)

begin

if (reset)

Sreg <= 16’b0;

Else if(enable)

For (i=15; i>=1;i=i-1)

Sreg [15] <= Sreg[i-1];

Sreg[0] <= data\_in;

End

…

**Question # 6 : [CLO-2, CLO-3,CLO-4]**

Write Verilog code of a module that contains four drivers that drive a single shared 1-bit output OUT in a half-duplex manner. When the select is 00, input of driver1 appears on OUT, when select is 01, input of driver2 appears on OUT, when select is 10, input of driver3 appears on OUT, otherwise input of driver3 appears on OUT. Attach simulation snaps of this code from Xilinx Vivado software. [20]

…

assign OUT = (select==2’b00): in1, 1’bz;

assign OUT = (select==2’b01): in1, 1’bz;

assign OUT = (select==2’b10): in2, 1’bz;

assign OUT = (select==2’b11): in3, 1’bz;

…

**Question # 7 : [CLO-1]**

Express difference between blocking and non-blocking assignments of Verilog HDL. Write a code in Verilog and synthesize it in Xilinx Vivado to show the effect of using the wrong assignment with the wrong construct. [10]

